Computer Science - 2 Most Likely Questions

1. (A) Select correct options and rewrite the following :

(a) Intel 8085 is a/an _____ bit Microprocessor.

(i) 16 (ii) 4 (iii) 8 (iv) 32

Ans. (iii) 8

(b) The instruction PCHL belongs to _____ group.

(i) Data transfer (ii) Logical (iii) Arithmetic (iv) Branching

Ans. (iv) Branching

(c) Stack pointer of 8085 holds _____.

(i) 8 bit address (ii) 16 bit data (iii) 16 bit address (iv) 8 bit data

Ans. (iii) 16 bit address

(d) The instruction set of intel 8051 Micro-controller contains total _____ instruction.

(i) 111 (ii) 72 (iii) 74 (iv) 100

Ans. (i) 111

(B) Answer any two of the following :

(a) Explain the function of following pins on Intel 8085 :

(i) $\overline{RD}$

Ans.
- This is read control signal. This is active low signal.
- This signal indicates that selected I/O or memory device is to be read and data is available on data bus.
- It is tristated during HOLD and HALT.

(ii) $\overline{WR}$

Ans.
- This is write control signal. This is also active low signal.
- This signal indicates that the data on data bus are to be written into selected memory or I/O locations.
- It is tristated during HOLD and HALT.

(iii) IO / $\overline{M}$

Ans.
- It is a status signal indicates whether the address bus is for I/O device or for memory.
- When it goes high, the address on the address bus refers I/O device and when it goes low, the address on the address bus refers memory.
- It is tristated during HOLD and HALT.

(b) Explain direct and immediate addressing modes of Intel 8085 with suitable examples.

Ans. **Direct addressing mode :**

(i) In direct addressing, the address appears after opcode of instruction in program memory.

(ii) The address of operand is specified within the instruction.

(iii) The instructions using direct addressing mode are three byte instructions. Byte 1 is opcode of instruction, Byte 2 is lower order address and Byte 3 is high order address.

(iv) For e.g. LDA 9FFFH

i.e. This instruction loads accumulator with content of memory location 9FFF H.

Immediate addressing mode :

(i) In Immediate addressing the data appears immediately after opcode of instruction in program memory.

(ii) In these instructions the actual data is specified within the instruction.

(iii) These operations are specified with either 2 or 3 byte instructions.

(iv) For e.g. ADI 05H

i.e. This instruction adds immediate data 05 H to the content of accumulator. The result is stored in accumulator.

(c) Explain any three important features of pentium processor.

Ans.

- Pentium is a 64 bit microprocessor, introduced in 1993.
- It has 64 bit data bus and 32-bit address bus. The use of super scalar architecture incorporates a dual- pipe lined processor, which lets and Pentium process more than one instruction per clock cycle.
- The addition both of data and code caches on chip is also a feature designed to improve processing speed.
- A new advanced computing technique used in Pentium is called the branch prediction, the Pentium makes an educated guess where the next instruction following a conditional instruction will be. This prevents instruction cache from running dry during conditional instructions.
- The pentium has 64-bit data bus. This means that it can perform data transfers with an external device twice as fast as a processor with a 32 bit data bus.

2. (A) **Answer any two of the following :**

(a) Write the RAM and ROM size of 8048, 8049 and 8050 Microcontrollers.

Ans. **8048, 8049, 8050**

(i) Intel's first microcontroller was 8048. The 8048, 8049 and 8050 all have indentical architectures with the exception of memory size.

(ii) In each case, the memory doubles. 8048 supports 1K byte of internal memory. 8049 supports 2k bytes of internal memory and 8050 supports 4K bytes of internal memory.

(iii) 8048 has 64 bytes internal RAM, including 32 bytes of register/memory location. The 8049 and 8050 have a total of 128 and 256 bytes of RAM respectively.

(iv) The microcontrollers are low cost products and hence are very popular.

(b) Explain Fiber-optic Cable with a neat diagram.

Ans.

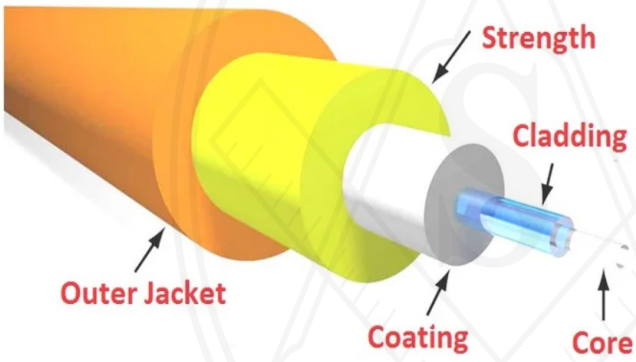
(i) The light wave can be efficiently conducted through transparent glass fiber cables known as optic fiber cables.

(ii) The centre conductor of this cable is a fibre that consists of highly refined glass or plastic.

(iii) It is designed to transmit light signals with little loss.

(iv) The fibre is coated with cladding or gel that reflects signals back into fibre to reduce signal loss. A plastic sheet protects the fibre from damage. This cable can carry much information at a time.

(v) The fibre optic cable is shown in following figure.



(vi) The fibre optic cable is used in optical transmission system.

(vii) This cable have extremely high bandwidth. It has zero sensitivity to EMI and runs over several kilometers.

The characteristics of fibre optic cable are given below

- **Cost** : The cost of fibre optic cable is more than that of co-axial cable and Twisted pair cable.
- **Installation** : Fibre optic cable requires skilled installation. Every cable has minimum bend radius. They may get damaged if bend sharply, Fibre optic cable can not be stretched.
- **Capacity** : Fibre optic cable supports high data rates (upto 2,00,000 MBPS), even with long run cables. Fibre optic cable can transmit 100 MBPS for several kilometer.
- **Attenuation** : Attenuation for fibre optic cable is much lower than co-axial cable and twisted pair cable. It can run to larger distance.
- **EMI** : Fibre optic cable does not use electrical signals to transmit data, therefore they are free from EMI. The data transfer in fibre optic cable have high security, as it can not be detected by electronic wave dropping equipments.

(c) Explain the conditional CALL instructions of Intel 8085.

Ans. **Conditional Call :** In conditional call, the subroutine is called only if the condition is satisfied. In conditional call, following procedure is followed, if the condition is true.

Format :

$$[[SP]-1] \leftarrow [PC_H]$$
$$[[SP]-2] \leftarrow [PC_L]$$
$$[SP] \leftarrow [SP]-2$$
$$[PC] \leftarrow \text{addr}$$

The conditional call instructions and conditions are as listed below:

(i) CC addr : Call if carry $(Cy = 1)$

(ii) CNC addr : Call if no carry $(Cy = 0)$

(iii) CZ addr : Call if zero $(Z = 1)$

(iv) CNZ addr : Call if no zero $(Z = 0)$

(v) CP addr : Call if plus $(S = 0)$

(vi) CM addr : Call if minus $(S = 1)$

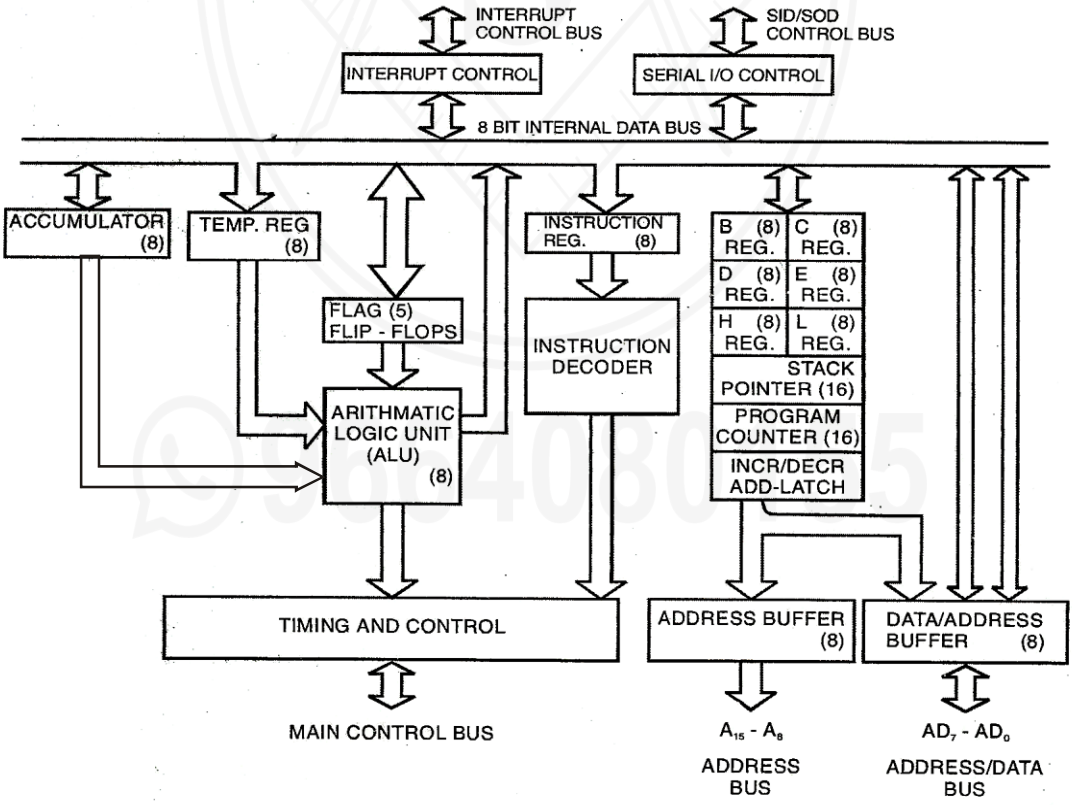
(vii) CPO addr : Call if odd parity $(P = 0)$

(viii) CPE addr : Call if even parity $(P = 1)$

(B) Answer any one of the following :

(a) Draw the functional block diagram of Intel 8085.

Ans.



Functional block diagram of Intel 8085

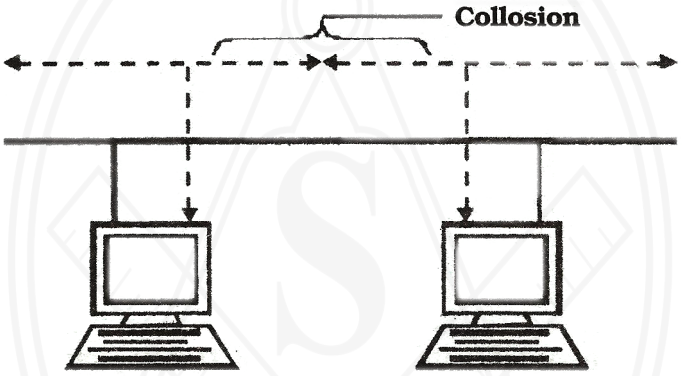
(b) Explain in brief the following access method :

(i) Contention

(ii) Token Passing

Ans. (i) **Contention**

- In contention, any computer in the network can transmit at any time (first come first served).
- This system breaks down when two computers attempt to transmit at the same time. This is a case of collision.
- To avoid collision, carrier sensing mechanism is used. Here each computer listens to the network before attempting to transmit. If network is busy, it waits until network quits down.
- In carrier detection, computers continue to listen to the network as they transmit. It computer detects another signal that interferes with the signal it is sending, it stops transmitting. Both computers then wait random amount of time and attempts to transmit.
- Contention methods are most popular media access control method on LANs.



(ii) **Token passing**

- Token passing utilize a frame called a token, which circulates around the network.
- A computer that needs to transmit must wait until it receives the token.
- When computer receives token, it is permitted to transmit.
- When computer completes transmitting, it passes the token frame to the next station or token ring network.

3. (A) **Answer any two of the following :**

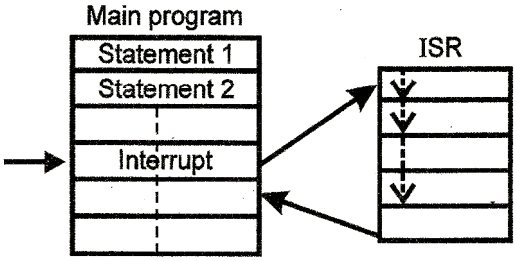
(a) What do you mean by Interrupt? List all the software interrupts of Intel 8085.

Ans. (i) An interrupt is a subroutine called, initiated by external device through hardware (hardware interrupt) or microprocessor itself (software interrupt).

(ii) An interrupt can also be viewed as a signal, which suspends the normal sequence of microprocessor and then microprocessor gives service to that device which has given the signal. After completing the service, microprocessor again returns to the main program.

(iii) Microprocessor is connected to different peripheral devices. To communicate with these devices, microprocessor 8085 uses interrupt method.

(iv) An interrupt is an input signal, which transfers control to specific routine known as Interrupt Service Routine (ISR). After executing ISR, control is again transfer to main program.



Software interrupt of Intel 8085:

- The normal operation of a microprocessor can be interrupted by special instruction. Such an interrupt is called a **Software interrupt.**
- 8085 provides 8 user defined software interrupts RST 0 to RST 7 where RST means restart.
- These interrupts are vectored interrupts and when these interrupts are called the control is transferred to the memory location as shown below:

Interrupt	Mnemonics	Call Location (Hex)
RST	0	0000H
RST	1	0008H
RST	2	0010H
RST	3	0018H
RST	4	0020H
RST	5	0028H
RST	6	0030H
RST	7	0038H

- Software interrupts are not used to handle asynchronous events. They are used to call software routines like single step, break point etc.
- These interrupts are requested by executing interrupt instructions. They can also be requested due to arithmetic errors.
- After execution of these interrupts, program counter is incremented. The microprocessor does not execute any interrupt acknowledge cycle. The microprocessor executes normal instruction cycle.
- These interrupts cannot be ignored or masked. They have more priority than any hardware interrupt.
- They are not used to interface peripherals. That means, they doesn't improve throughput of the system. They are used in program debugging.

(b) The Registers A and C of 8085 contain the data E2H and 47H. What will be the contents of Accumulator in Hex digits after execution of each of the following instructions independently ?

(i) SUB C

(ii) XRA C

(iii) ADD C

Ans. (i) $[A]=E2H$

$[C]=47H$

Instruction : SUB C

[C] = 47H = 0100 0111

2's complement of 47H is : 1011 1001 i.e. [B9H]

$$\begin{array}{r} 1011\,1001 \\ +[A]\ 1110\,0010 \\ \hline \boxed{1}\ 1001\,1011 \end{array}$$

After Execution: $[A]=9BH$

Carry [CY] = 00H

(ii) XRA C

$[A] = E2H = 11100010$

$[C] = 47H = 01000111$

$XRA\ C = 10100101$

$\therefore$ After execution : $[A]=A5H$

(iii) ADD C

$[A] = E2H = 11100010$

$[C] = 47H = 01000111$

$ADD\ C = \boxed{1}\ 00101001$

$\therefore$ After execution : $[A]=A9H$

Carry $[C_Y] = 01H$

(c) Draw a bit pattern of flag register of Intel 8085 and write the functions of any four flags.

Ans. (i) A flag is a single bit status register (Flip-Flop).

(ii) Flags are either set or reset by ALU according to the result by ALU.

(iii) Flags are important because they are the conditions for conditional branching instructions.

(iv) 8085 has five flags. Sign flag, Zero flag, Auxiliary Carry flag, Parity flag and Carry flag. A 8-bit register is used to represent five flags as shown in following figure:

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	——— Bit number
S	Z	-	Ac	-	P	-	Cy	——— Status flags

Where, S - Sign flag, Z - Zero flag, Ac- Auxiliary Carry flag, P - Parity flag, Cy-Carry flag.

- **Sign flag (S) :** After the execution of arithmetic and logic operation, if the most significant bit of the result is 1, then the sign flag is set to 1 otherwise 0.

  This flag is used with signed number. If MSB is 1, the number will be negative and if it is 0, the number will be positive.

- **Zero flag (Z):** After performing an arithmetic or logic operation, if the result is zero, then zero flag is set to 1, else it is reset. This flag is modified by the results in accumulator as well as in other registers.

- **Parity flag (P) :** Parity flag is set to 1, if the result stored in accumulator contains even parity. i.e. even number of 1's. If accumulator contains odd number of 1's, the flag is 0 i.e. Reset.

- **Carry flag (Cy) :** This flag sets if carry produced by most significant bit during the execution of an arithmetic operation. In subtraction carry flag serve as borrow flag.

(B) **Answer any one of the following :**

(a) Explain in brief the following connectivity devices :

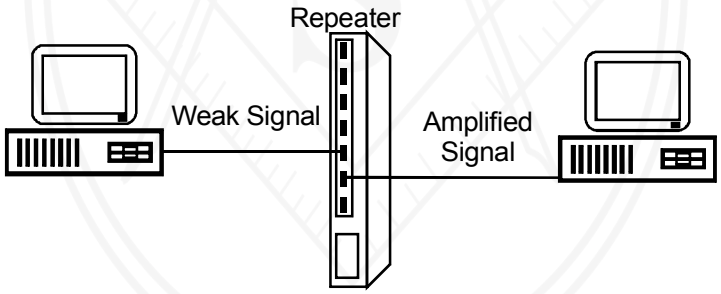
(i) Repeater

(ii) Router

Ans. **(i) Repeater**

- A repeater is a hardware unit mostly used in Ethernet to extend.
- A repeater reshapes and amplifies the signal from one Ethernet segment to another.

Figure shows network with repeaters



- A backbone cable runs vertical up in the building and a repeater is used to attach an Ethernet segment running in each floor of the office to the backbone cable.
- No two Ethernet workstations can have more than two repeaters between them, if they have to communicate reliably.
- The main disadvantage of repeaters is that they repeat noise in the system.
- Separate power supply is needed for repeaters.

(ii) Router

- Routers are internetwork connectivity devices. They are used to connect two topologically similar or dissimilar LANs. i.e. the LANs can be different e.g. they can be ethernet and token ring. Each LAN is logically separate and is assigned an address.
- Router can use network address to assist efficient delivery of message. Delivering packets according to logical network address to assist is called as routing. Routers performs routing.

- Router are intelligent. They can use algorithms to determine most efficient path for sending a packet to any given network.
- Router are also be used to divide large, busy LANs into smaller segments.
- Router are also employed to connect LAN to wide area network (WAN).
- Router are of two types:

  1. Static routers 2. Dynamic routers

  Static routers do not determine paths, but you need to specify them. Dynamic router have capacity to determine paths (routers).

(b) Define the terms - Machine Cycle, Instruction Cycle and T-state with a timing diagram.

Ans. **(i) Instruction cycle**

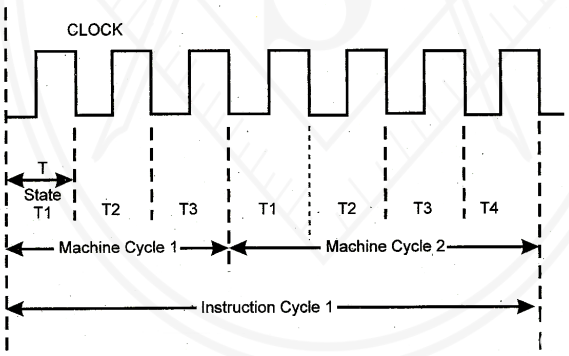
An instruction cycle is defined as the time required to complete the execution of an instruction. The 8085 instruction cycle consists of one to five machine cycle.

(ii) Machine cycle

Machine cycle is defined as the time required to complete any operation of accessing either memory or I/O which is the subpart of an instruction. In 8085, the machine cycle may consist of three to six T-states.

(iii) T-State

The subdivision of an operation, which is performed in one clock period is called as T-state. Diagrammatic representation is as follows:



The above diagram shows machine cycles, T-states and instruction cycle required for execution of an instruction. From above diagram it is clear that an instruction cycle consists of number of machine cycles and a machine cycle consists of number of T- states.

4. (A) **Answer any two of the following :**

(a) Explain the function of following instructions of Intel 8085 :

(i) $L \times I\ H$, 2900 H

(ii) LDA 6605 H

(iii) $PUSH\ B$

Ans. (i) *LXI H, 2900H* [LOAD REGISTER PAIR IMMEDIATE]

Format : LXI rp, addr
Addressing : Immediate
Group : Data transfer group
Bytes : 3 bytes
Flag : None

Comment: The byte 3 of instruction is moved into high order register (r_h) of register pair rp any byte 2 is moved into low order register (r_l) of register pair. The register pairs can be BC, DE, HL or SP. [SP (stack pointer) is not a valid register pair, but it can be used in LXI instruction]
Example : LXI H, 2900 H
This instruction will load H-L pair with 2900 H. 29 H will be loaded in high order register (H) and 00H will be loaded in low order register (L).

(ii) *LDA 6605H* [LOAD ACCUMULATOR DIRECT]

Format : [A] ← [[byte 3] [byte 2]]
Addressing : Direct addressing mode
Group : Data transfer group
Bytes : 3 bytes
Flag : None

Comment: This instruction will load accumulator with content of memory location, whose address is given in the instruction itself. The contents of memory location are not altered.
Example : Let [6605H] = 26 H
Instruction : LDA 6605H
After execution : [A] = 26 H
[6605H] = 26 H

(iii) *PUSH B* [PUSH REGISTER PAIR ON STACK]

Format : [[SP] - 1] ← [rh]
[[SP] - 2] ← [rl]
[SP] ← [SP] - 2
Addressing : Register indirect addressing
Bytes : 1 byte
Flags : None

Comment :
(a) The contents of the higher order register of register pair rp are moved to memory location, whose address is one less than the content of stack points.
(b) The contents of the low order register or register pair rp are moved of the memory location whose address is two less than the content of stack pointer.
(c) The stack pointer is determined by two. rp may be any one of the B (B & C), D (D & E), H (H & L)

Example: Let [SP] = D015 H, [B] = 25 H and [C] = 55 H

Instruction : PUSH B

After execution: [D014] = 25 H

[D013] = 55 H

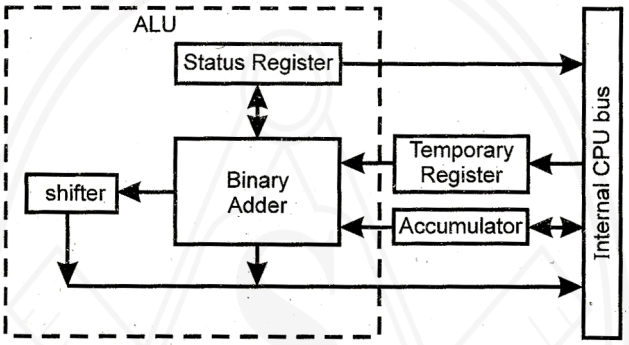
and [SP] = D013 H

Stack

SP →	D013	55
	D014	25
	D015	X

(b) Explain the function of ALU with a simple block diagram.

Ans. The organization of arithmetic and logic unit is shown in figure.



(i) The arithmetic and logic unit is 8-bit unit.

(ii) It performs arithmetic, logic and rotate operations.

(iii) It consists of binary adder to perform addition and subtraction by 2's complement method.

(iv) The result is typically stored in accumulator.

(v) Accumulator, temporary register and flag register are closely associated with A.L.U.

(vi) The temporary register is used to hold data during an arithmetic/ logic operation.

(vii) The flags are set or reset according to the result of operations in status register.

(c) What do you mean by Protocol ? Explain the concept of TCP/IP Protocol.

Ans. (i) A protocol is defined as an agreement between communication particle for how communication should be proceed.

OR protocols are rules by which computers communicates i.e. protocol is set of rules and formats for sending and receiving data.

(ii) Internet protocol are called TCP/IP (Transmission Control Protocol/Internet Protocol) protocols. This protocol do not belong to any one company and technology is available to everybody.

(iii) TCP/IP protocol use three types of addresses for network addressing

- Hardware or physical address is used by the data link and physical layers.
- Internet protocol address provides logical node identification. This address is unique address assigned by administratory expressed in four parts dotted notation. e.g. 123.144.131.21
- Logical node names are easier to remember than an IP address.

(B) Answer any one of the following :

(a) What is Microcontroller ? State any six important features of Intel 8051 Microcontroller.

Ans. **Microcontroller :** A microcontroller is a complete microprocessor system, consisting of microprocessor, limited amount of ROM or EPROM, RAM and I/O ports, built on a single integrated circuit.Microcontroller is infact a microcomputer, but it is called so because it is used to perform control functions.

The main features of 8051 are as listed below.

(i) The 8051 microcontroller has an 8-bit ALU.

(ii) The 8051 has 4K byte (4K × 8 bit) ROM or EPROM.

(iii) The 8051 has 128 byte (128 × 8 bit) RAM.

(iv) It has dual 16-bit timer event counter.

(v) It has 32 I/O lines for four 8-bit I/O ports.

(vi) It can address 64 kB of program memory.

(vii) It can address 64 kB of data memory.

(viii) It has powerful instruction set, consisting of 111 instructions.

(ix) It has two external interrupts.

(x) The 8051 has clock upto 12-MHz frequency.

(xi) Full-featured serial port.

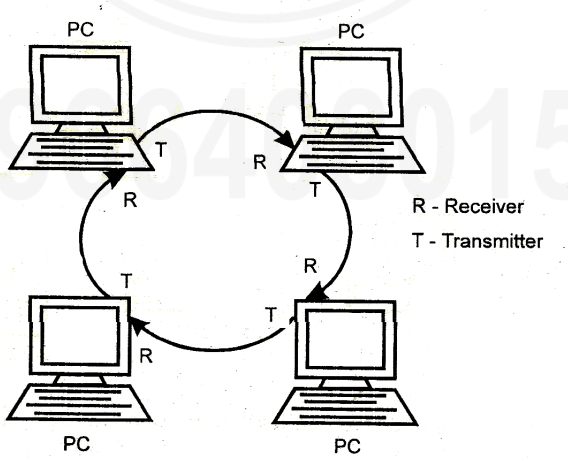
(b) Explain Ring and Star Topologies with simple diagrams.

Ans. **Ring Topology:**

(i) RING topologies are wired in a circle. Each node is connected to its neighbours on either side, and the data transmits along the ring in one direction only.

(ii) Each device incorporates a receiver and a transmitter and serves as a repeater that passes the signal onto the next device in the ring.

(iii) The RING topology is as shown in following figure:



(iv) RING topologies are suited for networks that uses token passing access methods. The token passes around the ring, and the only node that holds the token can transmit data.

(v) This topology is always implemented as a logical topology.

e.g. In token ring network, the topology is physically a STAR topology. But logical topology is RING topology.

(vi) The commonly used implementation for RING topology is token ring at 4-16 MBPS.

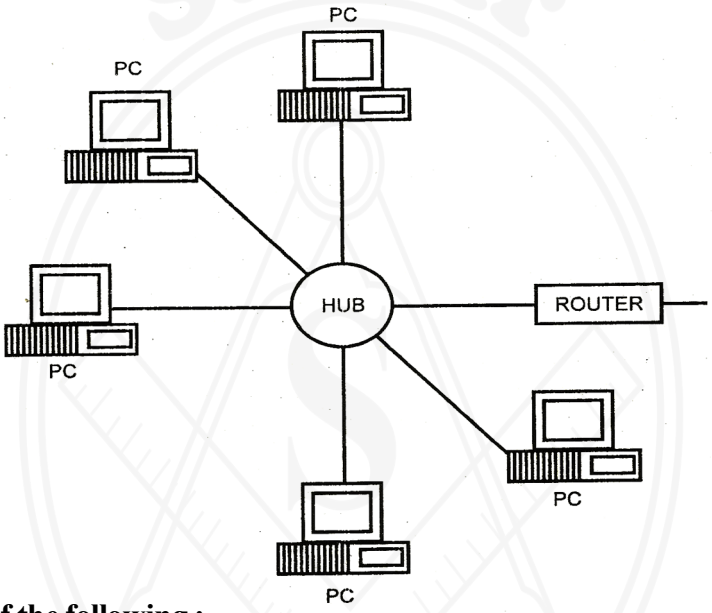
Star Topology:

(i) In a STAR topology all the workstations are connected to central hub.

(ii) The hub receives signal from a workstation and routes it to the proper destination.

(iii) STAR physical topology is often implemented to implement BUS or RING logical topology.

(iv) A STAR topology is shown in following figure:



5. Answer any two of the following :

(a) Write an Assembly Language Program to multiply an 8-bit number stored at 4301H by another 8-bit number stored at 4302H. Store the result at the location 4303H and 4304H beginning with LOB. (Lower Order Byte)

Ans.

Label	Mnemonics	Comment
	LXI H, 0000H	; Set initial product = 0
	LDA 4301H	; Set [Acc] = N1
	MOV E, A	; Set [E] = N1
	LDA 4302H	; Set [Acc] = N2
	MVI D, 00H	; Set [D] = 00H
Loop:	DAD D	; product = product + N1
	DCR A	; N2 = N2 – 1
	JNZ Loop	; Repeat, if N2 ≠ 0
	SHLD 4303H	; Store product in 4303H and 4304H
	RST 1.0	; Restart

(b) Write an Assembly Language Program to fill in the memory locations starting from 6900H an onward with the decimal numbers 0 to 99.

Ans.

Label	Mnemonics	Comment
START :	LXI H, 6900 H	; Load HL pair with 6900H
	MVI B, 64 H	; Store memory block count in B
	SUB A	; Clear accumulator
BACK :	MOV M, A	; Move accumulator to memory
	ADI 01H	; Add 01 to accumulator
	DAA	; Decimal adjust accumulator
	INX H	; Increment HL memory pointer
	DCR B	; Decrement counter by one
	JNZ BACK	; Jump, if no zero to BACK
	RST 1.0	; Restart

(c) Write an Assembly Language Program to take the 2's complement of an 8-bit number stored at 3301H. Store the result at the memory location 3302H.

Ans.

Label	Mnemonics	Comments
	LXI H, 3301H	; Load HL with 3301 H
	MOV A, M	; Get no. in Acc.
	CMA	; Complement given number
	INR A	; Increment A reg. By 1 to get 2's complement
	INX H	; Increment HL pair
	MOV M, A	; Place result in 3302 H
	RST 1.0	; Restart

OR

5. Answer any two of the following :

(a) Write an Assembly Language Program to count the occurrence of the data byte ACH in a memory Nock stored from 7401H to 7405H. Store the count at the memory location 7406H.

Ans.

Label	Mnemonic + Operand	Comments
START :	MVI C, 05H	; Store count 05H in register C
	MVI B, 00H	; Initialize occurrence count in register B
	LXI H, 7401H	; Initialize H-L pair with starting address
LOOP :	MOV A, M	; Get the number in accumulator
	CPI ACH	; Check whether the number in accumulator is ACH
	JNZ NEXT	; If no? jump to label NEXT
	INR B	; Yes, increment content in register B by 1
NEXT :	INX H	; Increment H-L pair
	DCR C	; Decrement count
	JNZ LOOP	; Is count zero? No-jump to label LOOP
	MOV A, B	; Get count in accumulator
	STA 7406H	; Store count of occurrence 7406H
END :	RST 1.0	; Restart

(b) Write a subroutine in assembly language to fill the memory locations 7301H to 73FFH with the hexa-decimal numbers 01H to FFH respectively.

Ans.

Label	Mnemonic	Comment
START :	LXI D, 7301H	; Set memory start address
	MVI A, 01 H	; Set accumulator to immediate data 01 H
	MVI B, FFH	; Load counter
LOOP :	STAX D	; Store data in memory
	INR A	; Increment data
	INR E	; Increment memory address
	DCR B	; count = count – 1
	JNZ LOOP	; go back if not over
	RET	; return to main program if over

(c) Write an Assembly Language Program to count the total number of even data bytes occuring in a block of data stored from 9201H to 920AH. Store the result (count) at the memory location 9500H.

Ans.

Label	Mnemonics	Comments
	MVI C, 00H	; Clear C reg
	MVI B, 0AH	; Set B = 0AH
	LXI H, 9201H	; Set HL = 9201 H
rep :	MOV A, M	; Get M to A
	RRC	; Rotate A to right
	JC next	; Jump, if carry to next
	INR C	; Increment C
next :	INX H	; Increment HL
	DCR B	; Decrement B
	JNZ rep	; Jump, if no zero to rep.
	MOV A, C	; Get C to A
	STA 9500H	; Store A at 9500 H
	RST 1.0	; Restart